What is claimed is:

1. A computer readable recording medium which records a wiring method for use in an automatic layout and wiring system, said medium recording:

a first program for reading information including a limit value of a predetermined wiring-facing length suitable for a short-run rule and an allowable short-run wiring space;

a second program for determining whether the short-run rule can be adapted when detected that a wiring space, between portions of wiring along grid lines of via cells which are parallel and adjacent to each other, is equal to or larger than the short-run wiring space, and setting, when determined that the short-run rule can be adapted, a via-margin changing flag indicating "change";

a third program for creating via cell data including a via margin which is so changed that the wiring space is equal to or larger than a wiring minimum space based on the via cells, when determined that the via-margin changing flag is set indicating "change" by said second program;

a fourth program for performing wiring of arrayed blocks and cells using the via cell data;

a fifth program for replacing the via cell data into art-work data corresponding to the via cells, after completion of the wiring.

2. The recording medium according to claim 1, wherein said first program includes:

a first step of determining whether to adapt the short-run rule while performing the wiring;

a second step of reading the short-run wiring space in accordance with the short-run rule, when determined that the short-run rule is to be adapted;

a third step of reading the limit value of the wiring-facing length according to the short-run rule;

a fourth step of obtaining a via-cell width by adding two times the via margin to a side length of a via;

a fifth step of determining whether the via-cell width is equal to or smaller than the limit value, and advancing to said second program when determined that the via-cell width is equal to or smaller than the limit value;

a sixth step of setting the via-margin changing flag indicating "no change", and advancing to said third program, when determined that the short-run rule is to be adapted in said first step or when determined that the via-cell width is not equal to or smaller than the limit value;

said second program including:

a seventh step of determining whether the via-cell width is larger than a standard wiring width suitable for signal wiring;

a eighth step of obtaining a logical minimum space by subtracting the via-cell width from a wiring space in accordance with a design rule when determined that the via-cell width is larger than the standard wiring width in said seventh step;

a ninth step of determining whether the logical minimum space is equal to or larger than the short-run wiring space;

a tenth step of setting the via-margin changing flag indicating "change" when determined that the logical minimum space is equal to or larger than the short-run wiring space, and advancing to said third program;

an eleventh step of setting the via-margin changing flag indicating "no change" when determined that the via-cell width is not larger than the standard wiring width in said seventh step or when the logical minimum space is not equal to or smaller

than the short-run wiring space in said ninth step, and advancing to said third program, and

said third program including:

a twelfth step of determining whether the via-margin changing flag is set indicating "change";

a thirteenth step of obtaining a virtual margin by performing a calculation, wherein the wiring minimum space according to the design rule is subtracted from the logical minimum space so as to obtain a value, the value is divided by two, and a quotient of the division is added to the via margin, when determined that the via-margin changing flag is set indicating "change" in said twelfth step;

a fourteenth step of changing the via margin into the obtained virtual margin; and

a fifteenth step of setting, when determined that the via-margin changing flag is not set indicating "change" in said twelfth step or after completion of said fourteenth step, a wiring margin while performing the wiring, and creating via cell data.

3. A computer readable recording medium which records a wiring method for use in an automatic layout and wiring system, said medium recording:

a first program for reading information including a limit value of a predetermined wiring-facing length suitable for a short-run rule and an allowable short-run wiring space;

a second program for determining that the short-run rule can be adapted, when a wiring space between a via cell and a portion of wiring along a grid line which is parallel and adjacent to the via cell is smaller than a wiring minimum space (long) and equal to or larger than the short-run wiring space, and setting a via-margin changing flag indicating "change";

a third program for creating via cell data including a via margin, which is so changed that the wiring space between the via cell and the portion of wiring is equal to or larger than the wiring minimum space, based on the via cell, when determined that the via-margin changing flag is set indicating "change" by said second program;

a fourth program for performing wiring of laid out blocks and cells using the created via cell data; and

a fifth program for replacing the via cell data with art-work data corresponding to the via cell after completion of the wiring.

4. The computer readable recording medium according to claim 3, wherein said first program includes:

a first step of determining whether to adapt the short-run rule while performing the wiring of the laid out blocks and cells;

a second step of reading the short-run wiring space according to the short-run rule, when determined that the short-run rule is to be adapted;

a third step of reading the limit value of the wiring-facing length in accordance with the short-run rule;

a fourth step of obtaining a via-cell width by adding two times the via margin to a side length of the via;

a fifth step of determining whether the via-cell width is equal to or smaller than the limit value, and advancing to said second program when determined that the via-cell width is equal to or smaller than the limit value;

a sixth step of setting the via-margin changing flag indicating "no change", when determined that the short-run rule is not to be adapted or when determined that the via-cell width is not equal to or smaller than the limit value, and advancing to said third program, and

said second program including:

a seventh step of determining whether the via-cell width is larger than a standard wiring width which is for signal wiring in accordance with a design rule;

an eighth step of obtaining a logical minimum space by performing a calculation, wherein the standard wiring width is added to the via-cell width so as to obtain a value, the value is divided by two, a quotient of the division is subtracted from a wiring pitch according to the design rule, when determined that the via-cell width is larger than the standard wiring width;

a ninth step of determining whether the logical minimum space is in a range between the short-run wiring space and the wiring minimum space;

a tenth step of setting the via-margin changing flag indicating "change", when determined that the logical minimum space is in the range, and advancing to said third program; and

an eleventh step of setting the via-margin changing flag "no change", when determined that the via-cell width is not larger than the standard wiring width in said seventh step or when determined that the logical minimum space is in the range in said ninth step, and advancing to said third program, and

said third program including:

a twelfth step of determining whether the via-margin changing flag is set indicating "change";

a thirteenth step of obtaining a virtual margin by performing a calculation, wherein the via margin is added to the logical minimum space so as to obtain a value, the wiring minimum space is subtracted from the obtained value, when determined that the via-margin changing flag is set indicating "change" in said twelfth step;

a fourteenth step of changing the via margin into the virtual margin; and

a fifteenth step of setting, when determined that the via-margin changing flag is not set indicating "change" in said twelfth step or after completion of said

fourteenth step, a wiring margin during the wiring of the laid out blocks and cells, and creating via cell data.

5. A layout and wiring system which automatically performs laying out and wiring of electronic components, comprising:

a detector which detects whether a space between a wiring pattern having a via cell and an adjacent wiring pattern is equal to or larger than a predetermined short-run wiring space;

a creator which creates, when detected that the space therebetween is equal to or larger than the predetermined short-run wiring space, via cell data including a via margin in such a way that a space between the via cell including the via margin and adjacent wiring is equal to or larger than a wiring minimum space; and

a drawer which performs laying out and wiring of the electronic components using the via cell data.

6. A system which automatically performs laying out and wiring of electronic components, comprising:

a detector which detects whether a space, between portions of wiring having via cells which are parallel and adjacent to each other, is equal to or larger than a short-run wiring space;

a creator which creates, when detected that the space therebetween is equal to or larger than the short-run wiring space, via cell data including a via margin which is changed based on the via cells in such a way that the wiring space is equal to or larger than a wiring minimum space; and

a controller which performs laying out and wiring of the electronic components using the via cell data.

7. An automatic layout and wiring system which automatically performs laying out and wiring of the electronic components in an grid having grid lines set at a predetermined wiring pitch, said system comprising:

a detector which detects that a space, between a via cell and a portion of wiring which is arranged along a grid line parallel and adjacent to a grid line of the via cell, is smaller than a wiring minimum space and equal to or larger than a short-run wiring space;

a creator which creates, when detected that the space therebetween is smaller than the wiring minimum space, via cell data including the via margin which is changed in such a way that the wiring space therebetween is equal to or larger than the wiring minimum space; and

a controller which performs laying out and wiring of the electronic components with the via cell data, and replaces the via cell data with art-work data corresponding to the via cell.